

TO THE ASSISTANT COMMISSIONER FOR PATENTS:

In the Drawings:

Please transfer FIGS. 1 – 2, 3B – 3D, and 4 – 13 from the file of the issued '070 patent to the reissue file.

Please amend FIGS. 3A and 3E as requested in the enclosed Request for Drawing Change.

In the Specification:

In Column 3, line 6, please replace "PG1 and PG2" with –[PG1 and PG2] IG1 and IG2–.

In Column 4, please replace with "RATIO  $\leq \frac{Tox_{ig}}{Tox_{pd}} \frac{W_{pd} / L_{pd}}{W_{ig} / L_{ig}} \frac{V_{cc} - V_{t_{ig}}}{V_{cc} - V_{t_{pd}}}$ " with

$$[RATIO \leq \frac{Tox_{ig}}{Tox_{pd}} \frac{W_{pd} / L_{pd}}{W_{ig} / L_{ig}} \frac{V_{cc} - V_{t_{ig}}}{V_{cc} - V_{t_{pd}}}]$$

$$RATIO \leq \frac{Tox_{ig}}{Tox_{pd}} \times \frac{W_{pd} / L_{pd}}{W_{ig} / L_{ig}} \times \frac{V_{cc} - V_{t_{pd}}}{V_{cc} - V_{t_{ig}}}$$

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In the Claims:

Please amend the claims as follows:

1. An SRAM memory cell comprising:
  - [a] first and second transfer gate transistors, the first transfer gate transistor having a first source/drain connected to a bit line and the second transfer gate transistor having a first source/drain connected to a complement bit line and each transfer gate transistor having a gate connected to a word line; [and]
  - first and second pull-down transistors configured as a storage latch, the first pull-down transistor having a first source/drain connected to a second source/ drain of said first transfer gate transistor and the second pull-down transistor having a first source/drain connected to a second source/drain of said second transfer gate